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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Nguyen et al.

Attorney Docket No.: NSC1P205D2

Patent: 6,838,317 B2

Issued: January 4, 2005

Title: TECHNIQUES FOR JOINING AN OPTO-ELECTRONIC MODULE TO A SEMICONDUCTOR PACKAGE

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on April 7, 2005 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: Tomika Thomas

Tomika Thomas

REQUEST FOR CERTIFICATE OF CORRECTION OF OFFICE MISTAKE (35 U.S.C. §254, 37 CFR §1.322)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Attn: Certificate of Correction

Dear Sir:

Attached is Form PTO-1050 (Certificate of Correction) at least one copy of which is suitable for printing. The errors together with the exact page and line number where they occur, and shown correctly in the application filed, are as follows:

SPECIFICATION:

1. Column 2, line 33, change "conductor" to --semiconductor--. This appears correctly in the patent application as filed on August 29, 2003, on page 3, line 4.

2. Column 7, line 37, change "pressure and beat" to --pressure and heat--. This appears correctly in the patent application as filed on August 29, 2003, on page 11, line 8.

Patentee hereby requests expedited issuance of the Certificate of Correction because the error lies with the Office and because the error is clearly disclosed in the records of the Office. As required for expedited issuance, enclosed is documentation that unequivocally supports the patentee's assertion without needing reference to the patent file wrapper.

It is noted that the above-identified errors were printing errors that apparently occurred during the printing process. Accordingly, it is believed that no fees are due in connection with the filing of this Request for Certificate of Correction. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. NSC1P205D2).

Respectfully submitted,
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(Also Form PT-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,838,317 B2

DATED : January 4, 2005

INVENTOR(S) : Nguyen et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the Specifications:

Column 2, line 33, change "conductor" to --semiconductor--.

Column 7, line 37, change "pressure and beat" to --pressure and heat--.

MAILING ADDRESS OF SENDER:

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PATENT NO. 6,838,317 B2

No. of Additional Copies

→ 1

TECHNIQUES FOR JOINING AN OPTO-ELECTRONIC MODULE TO A SEMICONDUCTOR PACKAGE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional of U.S. patent application Ser. No. 09/947,210, filed Sep. 4, 2001, now U.S. Pat. No. 6,642,613, which is a continuation-in-part of U.S. patent application Ser. No. 09/568,558, filed May 9, 2000, now U.S. Pat. No. 6,707,140, and a continuation-in-part of U.S. patent application Ser. No. 09/713,367, filed Nov. 14, 2000, now U.S. Pat. No. 6,497,518, U.S. patent application Ser. No. 09/947,210 claims the benefit of U.S. Provisional Application No. 60/331,377, filed Aug. 3, 2001.

This application is related to U.S. patent application Ser. No. 09/922,358, filed Aug. 3, 2001, and to U.S. patent application Ser. No. 10/412,564, filed Apr. 11, 2003.

U.S. patent application Ser. No. 09/922,358, U.S. patent application Ser. No. 09/568,558, and U.S. patent application Ser. No. 09/713,367, now U.S. Pat. No. 6,497,518, are hereby incorporated by reference.

FIELD OF THE INVENTION

The present invention relates to semiconductor packages, and more particularly, to a semiconductor package assembly that provides a true die to external fiber optic cable connection.

BACKGROUND OF THE INVENTION

Most computer and communication networks today rely on copper wiring to transmit data between nodes in the network. Since the data transmitted over the copper wire and the data processed within the nodes are both represented in the form of electrical signals, the transfer of data at the node-copper wire interface is straight forward. Other than perhaps a level shift and signal amplification, no other signal processing is required for data transmitted over the copper wire to be decoded by the node. The drawback with using copper wire is its relatively low bandwidth. Copper's ability to transmit data is significantly limited compared to other mediums, such as fiber optics. Accordingly much of the computer and communication networks being built today, including the Internet, are using fiber optic cabling instead of copper wire.

With fiber optic cabling, data is transmitted using light signals, not electrical signals. For example, a logical one may be represented by a light pulse of a specific duration and a logical zero may be represented by the absence of a light pulse for the same duration. In addition, it is also possible to transmit at the same time multiple colors of light over a single strand of optic fiber, with each color of light representing a distinct data stream. Since light is attenuated less in fiber than electrons traveling through copper, and multiple data streams can be transmitted at one time, the bandwidth of optic fiber is significantly greater than copper.

While fiber optic cabling is very efficient for transferring data, the use of light signals to process data is still very difficult. Data is typically transferred and stored in various locations before, during and after it is operated on in a computer. There still is no efficient way to "store" light signals representative of data. Networks will therefore likely continue using fiber optics for transmitting data between nodes and silicon chips to process the data within the nodes for the foreseeable future. The interface between the fiber optic cable and the nodes that process the data is therefore problematic because signals need to be converted between the electrical and the light domains.

Fiber optic transceivers, which convert light signals from a fiber optic cable into electrical signals, and vice versa, are used as the interface between a fiber optic line and a computer node. A typical transceiver includes a substrate, grooves etched in the substrate to receive the individual fiber optic strands, one or more semiconductor devices mounted on the substrate, one or more discrete optical detectors for converting light signals received over the fiber optic cables into electrical signals, one or more discrete optical emitters for converting electrical signals from the semiconductor devices into light signals. A number of fiber optic transceivers are commercially available from Hewlett Packard, AMP, Sumitomo, Nortel and Siemens. The problem with all of these fiber optic transceivers is that they are expensive and difficult to fabricate. With each transceiver, the semiconductor devices, emitters, and optical detectors have to be individually mounted onto the substrate, which is a costly and time consuming process. This limits the applications in which optical interconnects could be substituted for traditional copper usage. Furthermore the use of discrete emitters and optical detectors adversely affects the performance of the transceiver because electrical parasitics between discrete components are sources of electrical attenuation of inter-chip signals at Gigabit per second speeds that are generally used with such transceivers, more power is consumed for driving these traces than would not be needed for an integrated device. The form factor of the on-board optical transceiver is relatively large and therefore does not facilitate inter-board and chip-to-chip optical interconnectability.

A low cost conductor device that provides a true die to external fiber optic connection is therefore needed.

BRIEF SUMMARY OF THE INVENTION

The present invention provides a technique for manufacturing a low cost device that provides a true die to external fiber optic connection. Specifically, the present invention relates to several techniques for joining an optical device package to a semiconductor device package. The first technique involves using wirebond studs and an adhesive material, the second technique involves the use of an anisotropic conductive film, and the third technique involves the use of solder material. Each of these techniques provides high levels of thermal, electrical and optical performance. The methods apply to optical sub-assembly and chip sub-assembly interfaces in transceivers, transmitters, as well as receivers for opto-electronic packages.

One aspect of the present invention pertains to a method for attaching an optical device package to a semiconductor device package. This method includes forming a wirebond stud on an electrical contact surface located on a bottom surface of the optical device package and applying an adhesive material to the wirebond stud. Then the semiconductor device package is placed on the bottom of the optical device package such that an electrical contact surface on the semiconductor device package makes contact with the wirebond stud and the adhesive material applied to the wirebond stud. Then the adhesive material is cured so that the optical device package is firmly attached to the semiconductor device package.

In another aspect of the present invention, a method for attaching an optical device package to a semiconductor device package involves forming a wirebond stud on an electrical contact surface located on a bottom surface of the

consumed for driving these traces than would not be needed for an integrated device. The form factor of the on-board optical transceiver is relatively large and therefore does not facilitate inter-board and chip-to-chip optical interconnectability.

A low cost semiconductor device that provides a true die to external fiber optic connection is therefore needed.

interconnection interface between the OSA and the CSA. FIGS. 4A and 4B illustrate two types of particles. FIG. 4A illustrates a hard particle **400** for use in an anisotropic conductive film that has a hard nickel solid core **402** and a gold outer layer **404**. The hard particle **400** is intended to break through the oxide layer that typically forms on the surface of aluminum contact pads so that a good electrical contact can be formed. FIG. 4B illustrates a relatively soft particle **406** for use in an anisotropic conductive film that is made of a soft polymer shell **408** and a gold outer layer **410**. The relatively softer particle **406** is designed so that the polymer core collapses upon application of force, which allows for a smaller standoff gap between an OSA and a CSA. The ACF can contain only one type of conductive particle or it can contain a mixture of the two mentioned types of particles depending upon design parameters.

The technique of flow diagram **300** starts with block **302** where wirebond studs are formed on either the CSA or the OSA. In block **304**, an ACF is placed on an OSA if the wirebond studs were formed on a CSA, and an ACF is placed on a CSA if the wirebond studs were formed on an OSA. The process decision of placing the wirebond studs on the CSA or the OSA and the ACF on the respective OSA or CSA for attachment depends upon factors such as the assembly equipment parameters. For example, the pick and place mechanisms, the film handling mechanisms, the thermode configuration, etc., all can effect the decision. The chronological order of applying ACF and the application of wire ball studs is not important. These operations can be performed simultaneously. FIG. 5A illustrates a side plan view of an OSA **202** having an applied ACF **500** and a CSA **200** having wirebond studs **204**. On the other hand, FIG. 6A illustrates a side plan view of an OSA **202** having wirebond studs **204** and a CSA **200** having an applied ACF **500**.

In block **306**, the OSA and the CSA are placed together such that the wirebond studs **204** sink into the ACF **500**.

In block **308**, pressure and beat are applied to the OSA and CSA combination so that the wirebond studs **204** make contact with and apply pressure to the loose particles **502** within the ACF **500** so that the particles **502** make contact with each other. As a result, the particles **502** and the wirebond studs **204** provide an electrically conductive path between the electrical contact surfaces of the OSA **202** and the CSA **200**. FIG. 5B illustrates a side plan view of the OSA **202** and the CSA **200** of FIG. 5A after they have been placed together. Similarly, FIG. 6B illustrates a side plan view of the OSA **202** and the CSA **200** of FIG. 6A after they have been placed together. It is noted that since no gaps exist between the joined OSA and CSA, underfill is not required. The ACF can provide equivalent bonding support and heat dissipation qualities that underfill material provides. It is also noted that adhesive material does not need to be specifically applied to the wirebond studs since the ACF provides the adhering properties. After block **308** a separate curing process can be performed to cure the ACF material **500**. At this point the combination of the OSA and the CSA is completed. Due to the arrangement in which CSA's are aligned in a matrix array during manufacturing processes, it is preferable to apply the ACF to CSA rather than the OSA.

FIGS. 7A and 7B illustrate an alternative technique for use with ACF. FIG. 7A illustrates a side plan view of an OSA **202** having contact pads **700**, rather than wirebond studs, that will be placed onto a CSA **200** having a layer of ACF **500**. FIG. 7B illustrates a side plan view of the OSA **202** and the CSA **200** in FIG. 7A after they have been joined to each other. Heat and pressure are applied to the OSA and CSA combination to complete the joining technique. In alternative embodiments, the plates **700** can be attached to the CSA **200** and the ACF attached to the OSA **202**.

FIG. **8** illustrates a flow diagram **800** that represents the technique for attaching an OSA to a CSA by using solder material according to one embodiment of the present invention. FIGS. 9A–9C will be referenced and described throughout the description of FIG. **8** to facilitate the description of the solder attachment technique.

The solder technique of flow diagram **800** starts with block **802** where solder ball formations are applied to the electrical contact surfaces on the top of the CSA. Solder material can be applied to the CSA in various manners. First, solder wire material can be attached to the CSA through wire bonding technique where a solder wirebond stud is formed. The solder wirebond stud is then reflowed to form a solder ball formation. Secondly, solder paste can be screen printed directly onto the surface of the electrical contact surfaces of the CSA. The thickness of the solder material depends upon the thickness of the stencil and the size of the apertures within the stencil. Typically, stencils vary in thickness from 3 mils (minimum) and upward to 15 mils.

Another method is to dispense solder balls onto the electrical contact surfaces using a pressure-driven volumetric dispenser. Solder balls can also be placed on the CSA through the openings of a mesh placed on top of the CSA. Yet another method of applying solder balls onto the electrical contacts of a CSA is to place pre-formed solder balls onto the CSA. The size of the solder balls affects the standoff height between the CSA and the OSA. The solder balls have an initial height before the attachment of the OSA to the CSA and then they collapse to a shorter height after attachment.

FIG. 9A illustrates a side plan cross-sectional view of a CSA **900** having solder balls **902** formed on the electrical conduits **904** of the CSA **900**. The CSA **900** is a leadless leadframe package, which includes a die attach pad **906**, which supports a semiconductor die **908**. On top of the die **908** are the electrical conduits **904**, which can also be formed of solder material. Electrical contacts **912** are wirebonded to the die **908** and allow for the connection of the CSA **900** to an external device. The die attach pad **906**, the die **908**, the electrical contacts **912**, and the electrical conduits **904** are packaged within a plastic molding material **910**.

In block **804**, the solder material applied to the CSA in block **902** is reflowed to form the solder ball interface. In block **806**, flux is applied to the solder balls. As is commonly known, flux is applied to the surface of the solder balls to facilitate the flowing of the solder material and to prevent the formation of oxides.

In block **808**, an OSA **914** is placed on top of the solder balls **902** such that pads and electrical traces on the OSA that connect to the laser emitter **916** and the optical detector (not shown) of the OSA are connected to the electrical conduits **904** of the CSA **900** through solder balls **902**. FIG. 9B illustrates a side plan cross-sectional view of an OSA **914** placed on top of the solder balls **902** of the CSA **900**. The solder balls **902** make contact with pads and electrical traces connected to the laser emitter **916** and the optical detector of the OSA **914**.

In block **810**, the OSA and CSA combination undergoes a reflowing process to join the solder balls to the contacts on the OSA and the CSA, respectively. In block **812**, underfill material is injected into the interface between the OSA **914** and the CSA **900**. The underfill **900**, as described before, increases the strength of the bond between the OSA and the

chronological order of applying ACF and the application of wire ball studs is not important. These operations can be performed simultaneously. FIG. 5A illustrates a side plan view of an OSA 202 having an applied ACF 500 and a CSA 200 having wirebond studs 204. On the other hand, FIG. 6A illustrates a side plan view of an OSA 202 having wirebond studs 204 and a CSA 200 having an applied ACF 500.

In block 306, the OSA and the CSA are placed together such that the wirebond studs 204 sink into the ACF 500.

In block 308, pressure and heat are applied to the OSA and CSA combination so that the wirebond studs 204 make contact with and apply pressure to the loose particles 502 within the ACF 500 so that the particles 502 make contact with each other. As a result, the particles 502 and the wirebond studs 204 provide an electrically conductive path between the electrical contact surfaces of the OSA 202 and the CSA 200. FIG. 5B illustrates a side plan view of the OSA 202 and the CSA 200 of FIG. 5A after they have been placed together. Similarly, FIG. 6B illustrates a side plan view of the OSA 202 and the CSA 200 of FIG. 6A after they have been placed together. It is noted that since no gaps exist between the joined OSA and CSA, underfill is not required. The ACF can provide equivalent bonding support and heat dissipation qualities that underfill material provides. It is also noted that adhesive material does not need to be specifically applied to the wirebond studs since the ACF provides the adhering properties. After block 308 a separate curing process can be performed to cure the ACF material 500. At this point the combination of the OSA and the CSA is completed. Due to the arrangement in which CSA's are aligned in a matrix array during manufacturing processes, it is preferable to apply the ACF to CSA rather than the OSA.

FIGS. 7A and 7B illustrate an alternative technique for use with ACF. FIG. 7A illustrates a side plan view of an OSA 202 having contact pads 700, rather than wirebond studs, that will be placed onto a CSA 200 having a layer of ACF 500. FIG. 7B illustrates a side plan view of the OSA 202 and the CSA 200 in FIG. 7A after they have been joined to each other. Heat and pressure are applied to the OSA and CSA combination to complete the joining technique. In alternative embodiments, the plates 700 can be attached to the CSA 200 and the ACF attached to the OSA 202.

FIG. 8 illustrates a flow diagram 800 that represents the technique for attaching an OSA to a CSA by using solder material according to one embodiment of the present invention. FIGS. 9A-9C will be referenced and described throughout the description of FIG. 8 to facilitate the description of the solder attachment technique.